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EXAMINER	
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2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/509,201	MOON, SEUNG-HWAN	
	Examiner	Art Unit	
	JASON M. MANDEVILLE	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-7 and 10-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7 and 10-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 13 April 2009 has been entered.

Claim Objections

2. **Claim 2** is objected to because of the following informalities: the claim recites "the nth image data" in the last line of the claim." The claim should recite "the image data of the nth horizontal pixel line" to be consistent with the rest of the claim language. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-3, 5-7, and 11-15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Montalbo (US 6,356,260) in view of Sekido et al. (hereinafter "Sekido" US 2003 / 0048249) and further in view of Hiraki et al. (hereinafter "Hiraki" US 6,680,722).

5. As pertaining to **Claim 1**, Montalbo discloses (see Fig. 1 and Fig. 2) a liquid crystal display (see Col. 1, Ln. 14-18) comprising:

a liquid crystal panel assembly (10; see Fig. 1) including a plurality of gate lines (i.e., row lines), a plurality of data lines (i.e., column lines) which intersects the gate lines (i.e., row lines; see Col. 1, Ln. 19-48), and a plurality of pixels each of which is formed in an area defined by a data line (i.e., column line) of the data lines (i.e., column lines) and a gate line (i.e., row line) of the gate lines (i.e., row lines) and has a switching element (i.e., TFT) connected to the gate line (i.e., row line) and the data line (i.e., column line; again, see Col. 1, Ln. 19-48);

a gate driver (150) for supplying gate voltages (i.e., driving voltages) to the gate lines (i.e., row lines; again, see Col. 1, Ln. 19-48);

at least one data driver (see (120) of Fig. 1 corresponding to (200) of Fig. 2 corresponding to (320) of Fig. 3) for supplying data voltages corresponding to image data (i.e., pixel data) to the data lines (i.e., column lines; see Col. 1, Ln. 19-60); and

a timing controller (see (130) of Fig. 1 corresponding to (330) of Fig. 3 corresponding to (700) of Fig. 7) for comparing (see Fig. 7, for example) image data of an nth horizontal pixel line (i.e., current pixel data (710, 720) for a current line) in a frame applied from outside and image data of an (n-1)th horizontal pixel line (i.e., previous pixel data (722, 729) from a previous line) in the frame stored therein and selectively providing the image data of the nth horizontal pixel line (i.e., current pixel data (710, 720) for a current line) to the data driver (120, 200, 320) depending on the comparison result (see Col. 6, Ln. 34-65 in conjunction with Col. 8, Ln. 66-67 through Col. 9, Ln. 1-67 and Col. 10, Ln. 34-44; also see Col. Col. 6, Ln. 66-67 through Col. 7, Ln. 1-60), wherein the timing controller (130, 330, 700) does not provide the image data of the nth horizontal pixel line (i.e., current pixel data (710, 720) for the current line) to the data driver (120, 200, 320) when all bits of the image data of the nth horizontal pixel line (i.e., current pixel data (710, 720) for a current line) and the image data of the (n-1)th horizontal pixel line (i.e., previous pixel data (722, 729) from a previous line) are equal (i.e., the same; again, see Col. 6, Ln. 34-65 in conjunction with Col. 8, Ln. 66-67 through Col. 9, Ln. 1-67 and Col. 10, Ln. 34-44; also see Col. Col. 6, Ln. 66-67 through Col. 7, Ln. 1-60).

Montalbo does not explicitly disclose that the timing controller (130, 330, 700) also does not provide the image data of the nth horizontal pixel line (i.e., current image data (710, 720) of the current line) to the data driver (120, 200, 320) when all bits of the image data of the nth horizontal pixel line (i.e., current image data (710, 720) of the current line) and the image data of the (n-1)th horizontal pixel line (i.e., previous image data (722, 729) of the previous line) are complementary to each other. However, Montalbo does disclose that the primary goal of the invention is to reduce power consumption and electromagnetic interference by reducing the transfer of data from the timing controller to the data driver (see Col. 6, Ln. 34-65, for example).

Sekido discloses (see Fig. 1, Fig. 3, and Fig. 5) a liquid crystal panel assembly (1; see Fig. 1) including a plurality of gate lines (5), a plurality of data lines (6) which intersects the gate lines (5), and a plurality of pixels (3) each of which is formed in an area defined by a data line (6) of the data lines (6) and a gate line (5) of the gate lines (5) and has a switching element (i.e., TFT; 4) connected to the gate line (5) and the data line (6; see Page 2, Para. [0024]-[0025]). Further, Sekido discloses that the assembly comprises a gate driver (22; see Fig. 3) for supplying gate voltages to the gate lines (5) and at least one data driver (20; see Fig. 3) for supplying data voltages corresponding to image data to the data lines (see Page 3, Para. [0031] and [0034]). Sekido discloses a timing controller (implicit in (40, G1, G2; see Fig. 5) for comparing image data of an nth line (i.e., pixel data of the next pixel or line) applied from outside and image data of the (n-1)th line (i.e., pixel data of the previous pixel or line) stored therein and selectively

providing the image data of the nth line (i.e., pixel data of the next pixel or line) to the data driver (i.e., 20 in Fig. 3 corresponding to 30B, 32B, 34B, 36B, 38B of Fig. 5) depending on the comparison result (see Page 4, Para. [0042]-[0050]), wherein the timing controller (40, G1, G2; see Fig. 5) does not provide the image data of the nth line (i.e., pixel data of the next pixel or line) to the data driver (i.e., 20 in Fig. 3 corresponding to 30B, 32B, 34B, 36B, 38B of Fig. 5) when all bits of the image data of the nth line (i.e., pixel data of the next pixel or line) and the image data of the (n-1)th line (i.e., pixel data of the previous pixel or line) are complementary to each other (see Page 4, Para. [0049]-[0050]). Like Montalbo, Sekido discloses that the primary goal of the invention is to reduce power consumption and electromagnetic interference by reducing the transfer of data from a timing controller to a data driver (see Abstract and Page 1, Para. [0002]). Further, the inventions of Montalbo and Sekido are in the same field of endeavor. Therefore, it would have been obvious to one of ordinary skill in the art at the time when then invention was made to combine the teachings of Montalbo with the teachings of Sekido.

Furthermore, it would have been obvious to one of ordinary skill in the art at the time when the invention was made that the technique taught by Sekido, namely not providing the image data of the nth line to the data driver when all bits of the image data of the nth line and the image data of the (n-1)th line are complementary to each other, can be implemented in the timing controller of Montalbo. That is, implementing the teachings of Sekido in the timing controller of Montalbo constitutes the use of a known technique to improve a similar device in the same way.

In addition, while it is well known in the art that the gate lines and the data lines are insulated from each other, neither Montalbo nor Sekido explicitly state this feature. However, Hiraki discloses a liquid crystal display (see Fig. 3, Fig. 4, and Fig. 5) comprising: a liquid crystal panel assembly (40) including a plurality of gate lines (12), a plurality of data lines (13) which are insulated from and intersects the gate lines (12; see Col. 7, Ln. 48-53), and a plurality of pixels (herein referred to as picture elements) each of which is formed in an area defined by a data line (13) of the data lines (13) and a gate line (12) of the gate lines (12) and has a switching element (15) connected to the gate line (12) and the data line (13; Col. 7, Ln. 41-67). The teachings of Montalbo, Sekido, and Hiraki are in the same field of endeavor. Further, Hiraki provides a description of a feature common in liquid crystal displays. Therefore, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to combine the teachings of Montalbo, Sekido, and Hiraki.

6. As pertaining to **Claim 2**, the combined teachings of Montalbo and Sekido disclose (see Fig. 7 of Montalbo, for example) that the timing controller (see (130) of Fig. 1 corresponding to (330) of Fig. 3 corresponding to (700) of Fig. 7 of Montalbo) generates an operation control signal (i.e., see (752, 762, 772, 792) in Fig. 7 of Montalbo) based on the comparison result (i.e., the result of comparing the image data of the nth horizontal pixel line (i.e., current pixel data (710, 720) of the current line) applied from outside and image data of the (n-1)th horizontal pixel line (i.e., previous

pixel data (722, 729) of the previous line) as disclosed by Montalbo) and provides the operation control signal (i.e., see (752, 762, 772, 792) in Fig. 7 of Montalbo) to the data driver (see (120) of Fig. 1 corresponding to (200) of Fig. 2 corresponding to (320) of Fig. 3 of Montalbo) and the data driver (see (120) of Fig. 1 corresponding to (200) of Fig. 2 corresponding to (320) of Fig. 3 of Montalbo) is operated with a mode (see (740, 780) of Montalbo), based on the operation control signal (i.e., see (752, 762, 772, 792) in Fig. 7 of Montalbo), selected from a holding mode ((772, 792) of Montalbo) which provides data voltages corresponding to the stored image data of the (n-1)th horizontal pixel line (i.e., the previous pixel or line data as disclosed by Montalbo; again, see Col. 6, Ln. 34-65 in conjunction with Col. 8, Ln. 66-67 through Col. 9, Ln. 1-67 and Col. 10, Ln. 34-44; also see Col. Col. 6, Ln. 66-67 through Col. 7, Ln. 1-60), an inverting mode (i.e., (DINV) as disclosed by Sekido; see Fig. 5 of Sekido) which provides data voltages corresponding to the inverted image data of the (n-1)th horizontal pixel line (i.e., inverted pixel data of the previous pixel or line as disclosed by both Sekido and Montalbo; see Page 4, Para. [0049]-[0050] of Sekido), and an updating mode ((752) of Montalbo; see Fig. 7 of Montalbo) which provides data voltages corresponding to the image data of the nth horizontal pixel line (i.e., the current pixel or line data as disclosed by Montalbo) provided from the timing controller (see (130) of Fig. 1 corresponding to (330) of Fig. 3 corresponding to (700) of Fig. 7 of Montalbo; and again, see Col. 6, Ln. 34-65 in conjunction with Col. 8, Ln. 66-67 through Col. 9, Ln. 1-67 and Col. 10, Ln. 34-44; also see Col. Col. 6, Ln. 66-67 through Col. 7, Ln. 1-60 of Montalbo).

7. As pertaining to **Claim 3**, Montalbo and Sekido disclose (see Fig. 7 of Montalbo) that the timing controller (see (700) of Fig. 7 of Montalbo) can include:

a first line memory (see (710, 720) in Fig. 7 of Montalbo, for example) for storing the image data of the nth horizontal pixel line (i.e., the current line data) applied from outside;

a second line memory (see 722, 729 in Fig. 7 of Montalbo, for example) in which image data of the (n-1)th horizontal pixel line (i.e., the previous line data) applied in advance are stored (again, see Col. 6, Ln. 34-65 in conjunction with Col. 8, Ln. 66-67 through Col. 9, Ln. 1-67 and Col. 10, Ln. 34-44; also see Col. Col. 6, Ln. 66-67 through Col. 7, Ln. 1-60 of Montalbo); and

a control signal generator (see (752, 762, 772, 792 of Fig. 7 of Montalbo, for example) for generating the operation control signal (i.e., 752, 762, 772, 792) after comparing the image data of the nth horizontal pixel line (i.e., the current line data) and the image data of the (n-1)th horizontal pixel line (i.e., the previous line data; again, see Col. 6, Ln. 34-65 in conjunction with Col. 8, Ln. 66-67 through Col. 9, Ln. 1-67 and Col. 10, Ln. 34-44; also see Col. Col. 6, Ln. 66-67 through Col. 7, Ln. 1-60 of Montalbo), wherein

the control signal generator (see (752, 762, 772, 792 of Fig. 7 of Montalbo, for example) generates:

the operation control signal (792) of a first status (i.e., a hold status) to let the data driver (see (120) of Fig. 1 corresponding to (200) of Fig. 2 corresponding to (320) of Fig. 3 of Montalbo) operate with the holding mode (i.e., repeat last line) when all bits

of the image data of the nth horizontal pixel line (i.e., the current line data) and the image data of the (n-1)th horizontal pixel line (i.e., the previous line data) are equal to each other (again, see Col. 6, Ln. 34-65 in conjunction with Col. 8, Ln. 66-67 through Col. 9, Ln. 1-67 and Col. 10, Ln. 34-44; also see Col. Col. 6, Ln. 66-67 through Col. 7, Ln. 1-60 of Montalbo);

the operation control signal (i.e., (DINV) as disclosed by Sekido; see Fig. 5 of Sekido) of a second status (i.e., a hold and invert status) to let the data driver (see (120) of Fig. 1 corresponding to (200) of Fig. 2 corresponding to (320) of Fig. 3 of Montalbo) operate with the inverting mode when all bits of the image data of the nth horizontal pixel line (i.e., the current line data as disclosed by Sekido and Montalbo) and the image data of the (n-1)th horizontal pixel line (i.e., the previous line data as disclosed by Sekido and Montalbo) are complementary to each other (see Page 4, Para. [0049]-[0050] of Sekido); and

the operation control signal (i.e., (752); see Fig. 7 of Montalbo) of a third status (i.e., an update status) to let the data driver (see (120) of Fig. 1 corresponding to (200) of Fig. 2 corresponding to (320) of Fig. 3 of Montalbo) operate with the updating mode (i.e., video data output) when at least one bit of the image data of the nth horizontal pixel line (i.e., the current line data) and at least one corresponding bit of the image data of the (n-1)th horizontal pixel line (i.e., the previous line data) are not equal or complementary to each other (again, see Col. 6, Ln. 34-65 in conjunction with Col. 8, Ln. 66-67 through Col. 9, Ln. 1-67 and Col. 10, Ln. 34-44; also see Col. Col. 6, Ln. 66-67 through Col. 7, Ln. 1-60 of Montalbo);

8. As pertaining to **Claim 5**, both Montalbo and Sekido disclose (see Fig. 1, Fig. 2, and Fig. 7 of Montalbo; and see Fig. 2 and Fig. 5 of Sekido) that timing controller (see (130) of Fig. 1 corresponding to (330) of Fig. 3 corresponding to (700) of Fig. 7 of Montalbo) generates an operation control signal (i.e., see (792) of Fig. 7 of Montalbo; see (DINV) of Fig. 5 of Sekido) whose status changes by 1H period (i.e., one horizontal period) by comparing the image data of the nth horizontal pixel line (i.e., the current line pixel data) and the image data of the (n-1)th horizontal pixel line (i.e., the previous line pixel data) during 1H period (i.e., during one horizontal period) and the data driver (see (120) of Fig. 1 corresponding to (200) of Fig. 2 corresponding to (320) of Fig. 3 of Montalbo; see (20) in Fig. 3 corresponding to (30B, 32B, 34B, 36B, 38B) of Fig. 5 of Sekido) holds, inverts, or updates the image data by 1H period (i.e., by one horizontal period; see Col. 1, Ln. 19-48 and Col. 2, Ln. 8-20 in conjunction with again, see Col. 6, Ln. 34-65 in conjunction with Col. 8, Ln. 66-67 through Col. 9, Ln. 1-67 and Col. 10, Ln. 34-44; also see Col. Col. 6, Ln. 66-67 through Col. 7, Ln. 1-60 of Montalbo; i.e., the pixel data is held or updated at the data driver one horizontal line at a time; also see Page 2, Para. [0029]-[0030], Page 3, Para. [0032], [0036], and [0040], and Page 4, Para. [0042]-[0043] of Sekido).

9. As pertaining to **Claim 6**, both Montalbo and Sekido disclose (see Fig. 1, Fig. 2, and Fig. 6-8 of Montalbo; and see Fig. 2, Fig. 3 and Fig. 5 of Sekido) that timing controller (see (130) of Fig. 1 corresponding to (330) of Fig. 3 corresponding to (700) of

Fig. 7 of Montalbo) generates the operation control signal (i.e., see (752, 772, 792) of Fig. 7 of Montalbo; see (DINV) of Fig. 5 of Sekido) whose status changes as many times as the number of the data drivers (see (120) of Fig. 1 corresponding to (200) of Fig. 2 corresponding to (320) of Fig. 3 of Montalbo; see (20) in Fig. 3 corresponding to (30B, 32B, 34B, 36B, 38B) of Fig. 5 of Sekido) by 1H period (i.e., one horizontal period) by comparing the image data of the nth horizontal pixel line (i.e., the current line pixel data) and the image data of the (n-1)th horizontal pixel line (i.e., the previous line pixel data) for each data driver (see (120) of Fig. 1 corresponding to (200) of Fig. 2 corresponding to (320) of Fig. 3 of Montalbo; see (20) in Fig. 3 corresponding to (30B, 32B, 34B, 36B, 38B) of Fig. 5 of Sekido) during 1H period (i.e., during one horizontal period) and the data driver (see (120) of Fig. 1 corresponding to (200) of Fig. 2 corresponding to (320) of Fig. 3 of Montalbo; see (20) in Fig. 3 corresponding to (30B, 32B, 34B, 36B, 38B) of Fig. 5 of Sekido) holds, inverts, or updates the image data for each data driver (see Col. 1, Ln. 49-67 through Col. 2, Ln. 1-20 in conjunction with again, see Col. 6, Ln. 34-65 in conjunction with Col. 8, Ln. 66-67 through Col. 9, Ln. 1-67 and Col. 10, Ln. 34-44; also see Col. Col. 6, Ln. 66-67 through Col. 7, Ln. 1-60 of Montalbo and the above mentioned figures; also see Page 2, Para. [0029]-[0030], Page 3, Para. [0031]-[0035], and Page 4, Para. [0042]-[0046] of Sekido).

10. As pertaining to **Claim 7**, both Montalbo and Sekido disclose (see Fig. 1, Fig. 2, and Fig. 6-8 of Montalbo; and see Fig. 2, Fig. 3 and Fig. 5 of Sekido) that timing controller (see (130) of Fig. 1 corresponding to (330) of Fig. 3 corresponding to (700) of

Fig. 7 of Montalbo) generates an operation control signal (i.e., see (752, 772) of Fig. 7 of Montalbo; see (DINV) of Fig. 5 of Sekido) whose status changes as many times as the number of pixels of the line by 1H period (i.e., one horizontal period) by comparing the image data of the nth horizontal pixel line (i.e., the current line pixel data) and the image data of the (n-1)th horizontal pixel line (i.e., the previous line pixel data) for each pixel during 1H period (i.e., during one horizontal period) and the data driver (see (120) of Fig. 1 corresponding to (200) of Fig. 2 corresponding to (320) of Fig. 3 of Montalbo; see (20) in Fig. 3 corresponding to (30B, 32B, 34B, 36B, 38B) of Fig. 5 of Sekido) holds, inverts, or updates the image data for each pixel (see Col. 1, Ln. 19-48 through Col. 2, Ln. 1-20 in conjunction with again, see Col. 6, Ln. 34-65 in conjunction with Col. 8, Ln. 66-67 through Col. 9, Ln. 1-67 and Col. 10, Ln. 34-44; also see Col. Col. 6, Ln. 66-67 through Col. 7, Ln. 1-60 of Montalbo; also see Page 2, Para. [0029]-[0030], Page 3, Para. [0031]-[0035], and Page 4, Para. [0042]-[0050] of Sekido).

11. As pertaining to **Claim 11**, Montalbo discloses (see Fig. 3c) that the image data is transmitted to the data driver by RSDS (reduced swing differential signaling; see Abstract and Col. 5, Ln. 40-51).

12. As pertaining to **Claim 12**, Montalbo discloses (see Fig. 1 and Fig. 2) a driving method of a liquid crystal display (see Col. 1, Ln. 14-18) which includes a plurality of gate lines (i.e., row lines), a plurality of data lines (i.e., column lines) which intersects the gate lines (i.e., row lines; see Col. 1, Ln. 19-48), and a plurality of pixels each of

which is formed in an area defined by a data line (i.e., column line) of the data lines (i.e., column lines) and a gate line (i.e., row line) of the gate lines (i.e., row lines) and has a switching element (i.e., TFT) connected to the gate line (i.e., row line) and the data line (i.e., column line; again, see Col. 1, Ln. 19-48), the method comprising:

providing (see (120) of Fig. 1 corresponding to (200) of Fig. 2 corresponding to (320) of Fig. 3) data voltages according to image data (i.e., pixel data) to the data line (i.e., column line; see Col. 1, Ln. 19-60);

making the data voltage be applied to the pixel by providing (see (150)) a gate voltage (i.e., driving voltage) to the gate line (i.e., row line; again, see Col. 1, Ln. 19-48);

wherein the provision of data voltages includes:

comparing (see (130) of Fig. 1 corresponding to (330) of Fig. 3 corresponding to (700) of Fig. 7) image data of the (n-1)th horizontal pixel line (i.e., previous pixel or line data (722, 729)) in a frame provided in advance and image data of the nth horizontal pixel line (i.e., current pixel or line data (710, 720)) in the frame being provided currently (see (740, 780), for example; also see Col. 6, Ln. 34-65 in conjunction with Col. 8, Ln. 66-67 through Col. 9, Ln. 1-67 and Col. 10, Ln. 34-44; also see Col. Col. 6, Ln. 66-67 through Col. 7, Ln. 1-60);

providing data voltages corresponding to the image data of the (n-1)th horizontal pixel line (i.e., previous pixel or line data (722, 729)) to the data line (i.e., column line) when all bits of the image data of the nth horizontal pixel line (i.e., current pixel or line data (710, 720)) and the image data of the (n-1)th horizontal pixel line (i.e., previous pixel or line data (722, 729)) are equal to each other (again, see Col. 6, Ln. 34-65 in

conjunction with Col. 8, Ln. 66-67 through Col. 9, Ln. 1-67 and Col. 10, Ln. 34-44; also see Col. Col. 6, Ln. 66-67 through Col. 7, Ln. 1-60); and

providing data voltages corresponding to the image data of the nth horizontal pixel line (i.e., current pixel or line data (710, 720)) to the data line (i.e., column line) when at least one bit of the image data of the nth horizontal pixel line (i.e., current pixel or line data (710, 720)) and at least one corresponding bit of the image data of the (n-1)th horizontal pixel line (i.e., previous pixel or line data (722, 729)) are not equal to each other (again, see Col. 6, Ln. 34-65 in conjunction with Col. 8, Ln. 66-67 through Col. 9, Ln. 1-67 and Col. 10, Ln. 34-44; also see Col. Col. 6, Ln. 66-67 through Col. 7, Ln. 1-60); and

Montalbo does not explicitly disclose inverting the image data of the (n-1)th horizontal pixel line (i.e., the previous image data) and providing data voltages corresponding thereto when all bits of the image data of the nth horizontal pixel line (i.e., the current image data) and the image data of the (n-1)th horizontal pixel line (i.e., the previous image data) are complementary to each other. Moreover, Montalbo does not explicitly state providing data voltages corresponding to the image data of the nth horizontal pixel line (i.e., current pixel or line data (710, 720)) to the data line (i.e., column line) when at least one bit of the image data of the nth horizontal pixel line (i.e., current pixel or line data (710, 720)) and at least one bit of the image data of the (n-1)th horizontal pixel line (i.e., previous pixel or line data (722, 729)) are not complementary to each other. However, Montalbo does disclose that the primary goal of the invention

is to reduce power consumption and electromagnetic interference by reducing the transfer of data from the timing controller to the data driver (see Col. 6, Ln. 34-65).

Sekido discloses (see Fig. 1, Fig. 3, and Fig. 5) a method of driving a liquid crystal panel assembly (1; see Fig. 1) including a plurality of gate lines (5), a plurality of data lines (6) which intersects the gate lines (5), and a plurality of pixels (3) each of which is formed in an area defined by a data line (6) of the data lines (6) and a gate line (5) of the gate lines (5) and has a switching element (i.e., TFT; 4) connected to the gate line (5) and the data line (6; see Page 2, Para. [0024]-[0025]). Further, Sekido discloses that the assembly comprises a gate driver (22; see Fig. 3) for supplying gate voltages to the gate lines (5) and at least one data driver (20; see Fig. 3) for supplying data voltages corresponding to image data to the data lines (see Page 3, Para. [0031] and [0034]). Sekido discloses a timing controller (implicit in (40, G1, G2; see Fig. 5) for comparing image data of the nth line (i.e., pixel data of the next pixel or line) applied from outside and image data of the (n-1)th line (i.e., pixel data of the previous pixel or line) stored therein and selectively providing the image data of the nth line (i.e., pixel data of the next pixel or line) to the data driver (i.e., 20 in Fig. 3 corresponding to 30B, 32B, 34B, 36B, 38B of Fig. 5) depending on the comparison result (see Page 4, Para. [0042]-[0050]), wherein the timing controller (40, G1, G2; see Fig. 5) provides for inverting the image data of the (n-1)th line (i.e., the pixel data of the previous pixel or line) and providing data voltages corresponding thereto when all bits of the image data of the nth line (i.e., pixel data of the next pixel or line) and the image data of the (n-1)th line (i.e., pixel data of the previous pixel or line) are complementary to each other (see

Page 4, Para. [0049]-[0050]); and providing data voltages corresponding to the image data of the nth line (i.e., pixel data of the next pixel or line) to the data line when at least one bit of the image data of the nth line (i.e., pixel data of the next pixel or line) and at least one corresponding bits of the image data of the (n-1)th line (i.e., pixel data of the previous pixel or line) the previous image data) are not complementary to each other (again, see Page 4, Para. [0042]-[0050]). Like Montalbo, Sekido discloses that the primary goal of the invention is to reduce power consumption and electromagnetic interference by reducing the transfer of data from a timing controller to a data driver (see Abstract and Page 1, Para. [0002]). Further, the inventions of Montalbo and Sekido are in the same field of endeavor. Therefore, it would have been obvious to one of ordinary skill in the art at the time when then invention was made to combine the teachings of Montalbo with the teachings of Sekido.

Furthermore, it would have been obvious to one of ordinary skill in the art at the time when the invention was made that the technique taught by Sekido, namely not providing the image data of the nth horizontal pixel line to the data driver when all bits of the image data of the nth horizontal pixel line and the image data of the (n-1)th horizontal pixel line are complementary to each other, can be implemented in the timing controller of Montalbo. That is, implementing the teachings of Sekido in the timing controller of Montalbo constitutes the use of a known technique to improve a similar device in the same way. As such, the combined teachings of Montalbo and Sekido disclose providing data voltages corresponding to the image data of the nth horizontal pixel line to the data line when at least one bit of the image data of the nth horizontal

pixel line and at least one corresponding bit of the image data of the (n-1)th horizontal pixel line are not equal or complementary to each other.

In addition, while it is well known in the art that the gate lines and the data lines are insulated from each other, neither Montalbo nor Sekido explicitly state this feature. However, Hiraki discloses a liquid crystal display (see Fig. 3, Fig. 4, and Fig. 5) comprising: a liquid crystal panel assembly (40) including a plurality of gate lines (12), a plurality of data lines (13) which are insulated from and intersects the gate lines (12; see Col. 7, Ln. 48-53), and a plurality of pixels (herein referred to as picture elements) each of which is formed in an area defined by a data line (13) of the data lines (13) and a gate line (12) of the gate lines (12) and has a switching element (15) connected to the gate line (12) and the data line (13; Col. 7, Ln. 41-67). The teachings of Montalbo, Sekido, and Hiraki are in the same field of endeavor. Further, Hiraki provides a description of a feature common in liquid crystal displays. Therefore, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to combine the teachings of Montalbo, Sekido, and Hiraki.

13. As pertaining to **Claim 13**, both Montalbo and Sekido disclose (see Fig. 1, Fig. 2, and Fig. 7 of Montalbo; and see Fig. 2 and Fig. 5 of Sekido) that the provision compares the image data of the nth horizontal pixel line (i.e., the current line pixel data) and the image data of the (n-1)th horizontal pixel line (i.e., the previous line pixel data) during 1H period (i.e., during one horizontal period; see Col. 1, Ln. 19-48 and Col. 2, Ln. 8-20

in conjunction with again, see Col. 6, Ln. 34-65 in conjunction with Col. 8, Ln. 66-67 through Col. 9, Ln. 1-67 and Col. 10, Ln. 34-44; also see Col. Col. 6, Ln. 66-67 through Col. 7, Ln. 1-60 of Montalbo; i.e., the pixel data is held or updated at the data driver one horizontal line at a time; also see Page 2, Para. [0029]-[0030], Page 3, Para. [0032], [0036], and [0040], and Page 4, Para. [0042]-[0043] of Sekido).

14. As pertaining to **Claim 14**, both Montalbo and Sekido disclose (see Fig. 1, Fig. 2, and Fig. 6-8 of Montalbo; and see Fig. 2, Fig. 3 and Fig. 5 of Sekido) that the provision compares the image data of the nth horizontal pixel line (i.e., the current line pixel data) and the image data of the (n-1)th horizontal pixel line (i.e., the previous line pixel data) for each data driver (see (120) of Fig. 1 corresponding to (200) of Fig. 2 corresponding to (320) of Fig. 3 of Montalbo; see (20) in Fig. 3 corresponding to (30B, 32B, 34B, 36B, 38B) of Fig. 5 of Sekido) of the liquid crystal display during 1H period (i.e., during one horizontal period; see Col. 1, Ln. 49-67 through Col. 2, Ln. 1-20 in conjunction with again, see Col. 6, Ln. 34-65 in conjunction with Col. 8, Ln. 66-67 through Col. 9, Ln. 1-67 and Col. 10, Ln. 34-44; also see Col. Col. 6, Ln. 66-67 through Col. 7, Ln. 1-60 of Montalbo and the above mentioned figures; also see Page 2, Para. [0029]-[0030], Page 3, Para. [0031]-[0035], and Page 4, Para. [0042]-[0046] of Sekido).

15. As pertaining to **Claim 15**, both Montalbo and Sekido disclose (see Fig. 1, Fig. 2, and Fig. 6-8 of Montalbo; and see Fig. 2, Fig. 3 and Fig. 5 of Sekido) that the provision compares the image data of the nth horizontal pixel line (i.e., the current line pixel data)

and the image data of the (n-1)th horizontal pixel line (i.e., the previous line pixel data) for each pixel during 1H period (i.e., during one horizontal period; see Col. 1, Ln. 19-48 through Col. 2, Ln. 1-20 in conjunction with again, see Col. 6, Ln. 34-65 in conjunction with Col. 8, Ln. 66-67 through Col. 9, Ln. 1-67 and Col. 10, Ln. 34-44; also see Col. Col. 6, Ln. 66-67 through Col. 7, Ln. 1-60 of Montalbo; also see Page 2, Para. [0029]-[0030], Page 3, Para. [0031]-[0035], and Page 4, Para. [0042]-[0050] of Sekido).

16. **Claim 10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Montalbo in view of Sekido in view of Hiraki and further in view of Terukina et al. (hereinafter "Terukina" US 6,624,868).

17. As pertaining to **Claim 10**, Montalbo discloses that typical display driver circuit chips are mounted on the glass of the liquid crystal display panel (see Col. 1, Ln. 36-38). While chip on glass (COG) structures are well known in liquid crystal displays, none of Montalbo, Sekido, nor Hiraki explicitly state that the liquid crystal display has a COG (chip on glass) structure.

However, Terukina discloses a liquid crystal display with a chip-on-glass (COG) structure (see Fig. 4) in which the chips for driving the liquid crystal display panel are mounted on a glass substrate (Col. 1, Ln. 14-45). Terukina explicitly states that COG structures are well known in the art (see Col. 1, Ln. 7-19). Therefore, it would have been obvious to one of ordinary skill in the art at the time when the invention was made

to combine the teachings of Montalbo, Sekido, and Hiraki with the teachings of Terukina as a means of applying a known technique (i.e., the COG structure) to a known device (i.e., a liquid crystal display) to yield predictable results (i.e., the improvements disclosed by Terukina; see Col. 1, Ln. 34-64).

Response to Arguments

18. Applicant's arguments filed 13 April 2009 have been fully considered but they are not persuasive. **Claims 1-3, 5-7, and 10-15** are pending in the application. The applicant has argued that none of the references relied upon in the prior office action, namely Montalbo (US 6,356,260), Sekido et al. (US 2003 / 0048249), Hiraki et al. (US 6,680,722), and Terukina et al. (US 6,624,868), teach or fairly suggest "a timing controller for comparing image data of an nth horizontal pixel line applied from outside and image data of an (n-1)th horizontal pixel line stored therein...." The examiner respectfully disagrees for the reasons provided in the above rejections. In particular, the examiner would like to point out that Montalbo discloses exactly such a timing controller with respect to Fig. 7, wherein image data of an nth horizontal pixel line is compared with image data of an (n-1)th horizontal pixel line. Therefore, the rejection of **Claims 1-3, 5-7, and 10-15** is maintained.

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON M. MANDEVILLE whose telephone number is 571-270-3136. The examiner can normally be reached on Monday through Friday 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander Eisen can be reached on 571-272-7687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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